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Department of Physics and Electronics

Name of the course— B.Sc. (H) Physics

Semester- IV

Name of the paper—Electrical circuits and Network Skills

Paper code-32223903

Lecture Time-- Saturday (10:40 to 12:40)

Topics to be covered:

Unit-2

Electrical Circuits: Basic electric circuit elements and their combination. Rules to analyze DC sourced electrical circuits. Current and voltage drop across the DC circuit elements. Single-phase and three-phase alternating current sources. Rules to analyze AC sourced electrical circuits. Real, imaginary and complex power components of AC source. Power factor. Saving energy and money.

Unit-6

Resistors, inductors and capacitors. Diode and rectifiers. Components in Series or in shunt. Response of inductors and capacitors with DC or AC sources

Power absorbed by a load

Considerable effort has been expended over the years to express power relations as simply as possible. Power engineers have coined the term complex power, which they use to find the total effect of parallel loads.

Complex power is important in power analysis because it contains all the information pertaining to the power absorbed by a given load.

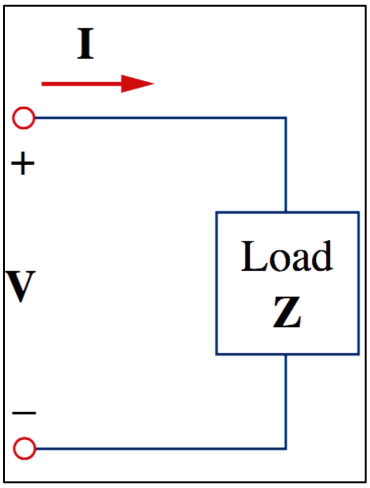


Figure 1

Consider the AC load in Figure 1 above. Given the phasor form $V = V_m\angle\theta_v$ and $I = I_m\angle\theta_i$ of voltage v(t) and current i(t), the complex power S absorbed by the AC load is the product of the voltage and the complex conjugate of the current, or:

$$\mathbf{S} = \frac{1}{2}\mathbf{V}\mathbf{I}^* \tag{2.1}$$

When you write in terms of rms value:

$$\mathbf{S} = \mathbf{V}_{\text{rms}}\mathbf{I}^*_{\text{rms}} \tag{2.2}$$

Where

$$\mathbf{V}_{\text{rms}} = \frac{\mathbf{V}}{\sqrt{2}} = V_{\text{rms}}\underline{/\theta_v} \tag{2.3}$$

Thus we may write Eq. (1.11) as:

$$\begin{aligned}\mathbf{S} &= V_{\text{rms}}I_{\text{rms}}\underline{/\theta_v - \theta_i} \\ &= V_{\text{rms}}I_{\text{rms}}\cos(\theta_v - \theta_i) + jV_{\text{rms}}I_{\text{rms}}\sin(\theta_v - \theta_i)\end{aligned} \tag{2.4}$$

The complex power may be expressed in terms of the load impedance Z. The load impedance Z may be written as:

$$\mathbf{Z} = \frac{\mathbf{V}}{\mathbf{I}} = \frac{\mathbf{V}_{\text{rms}}}{\mathbf{I}_{\text{rms}}} = \frac{V_{\text{rms}}}{I_{\text{rms}}} \underline{/\theta_v - \theta_i}$$

(2.5)

Thus, $V_{rms} = Z \times I_{rms}$. Substituting this into Eq. (1.11) gives

$$\boxed{\mathbf{S} = I_{\text{rms}}^2 \mathbf{Z} = \frac{V_{\text{rms}}^2}{\mathbf{Z}^*} = \mathbf{V}_{\text{rms}} \mathbf{I}_{\text{rms}}^*}$$

(2.6)

Since Z = R + jX, Eq. (1.16) becomes

$$\mathbf{S} = I_{\text{rms}}^2 (R + jX) = P + jQ$$

(2.7)

where P and Q are the real and imaginary parts of the complex power; that is,

$$P = \text{Re}(\mathbf{S}) = I_{\text{rms}}^2 R$$

$$Q = \text{Im}(\mathbf{S}) = I_{\text{rms}}^2 X$$

(2.8, 2.9)

"P is the average or real power and it depends on the load's resistance R. Q depends on the load's reactance X and is called the reactive (or quadrature) power."

Comparing Eq. (1.14) with Eq. (1.17), we notice that:

$$P = V_{\text{rms}} I_{\text{rms}} \cos(\theta_v - \theta_i), \qquad Q = V_{\text{rms}} I_{\text{rms}} \sin(\theta_v - \theta_i)$$

(2.10)

The real power P is the average power in watts delivered to a load. It is the only useful power. It is the actual power dissipated by the load. The reactive power Q is a measure of the energy exchange between the source and the reactive part of the load.

The unit of Q is the volt-ampere reactive (VAR) to distinguish it from the real power, whose unit is the watt.

Notice that:

1. **Q = 0** for resistive loads (unity pf)
2. **Q < 0** for capacitive loads (leading pf)

3. **Q > 0** for inductive loads (lagging pf)

Thus,

Complex power (in VA) is the product of the rms voltage phasor and the complex conjugate of the rms current phasor. *As a complex quantity, its real part is real power P and its imaginary part is reactive power Q.*

Introducing the complex power enables us to obtain the real and reactive powers directly from voltage and current phasors.

$$\text{Complex Power} = \mathbf{S} = P + jQ = \mathbf{V}_{\text{rms}}(\mathbf{I}_{\text{rms}})^* = V_{\text{rms}} I_{\text{rms}} \underline{/\theta_v - \theta_i}$$

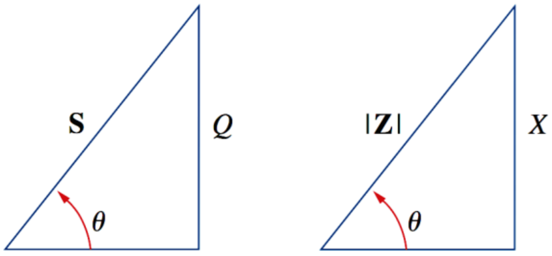
$$\text{Apparent Power} = S = |\mathbf{S}| = V_{\text{rms}} I_{\text{rms}} = \sqrt{P^2 + Q^2}$$

$$\text{Real Power} = P = \text{Re}(\mathbf{S}) = S\cos(\theta_v - \theta_i)$$

$$\text{Reactive Power} = Q = \text{Im}(\mathbf{S}) = S\sin(\theta_v - \theta_i)$$

$$\text{Power Factor} = \frac{P}{S} = \cos(\theta_v - \theta_i)$$

This shows how the complex power contains all the relevant power information in a given load. It is a standard practice to represent **S, P, and Q in the form of a triangle, known as the power triangle**, shown in Fig. 2(a). This is similar to the impedance triangle showing the relationship between Z, R, and X, illustrated in Fig.



(a) (b)

Figure 2

S contains all power information of a load. The real part of S is the real power P. Its imaginary part is the **reactive power Q**. Its magnitude is the **apparent power S**. And the cosine of its phase angle is the **power factor PF**.

The power triangle has four items:

1. Apparent/complex power,
2. Real power,
3. Reactive power, and
4. Power factor angle.

Given two of these items, the other two can easily be obtained from the triangle.

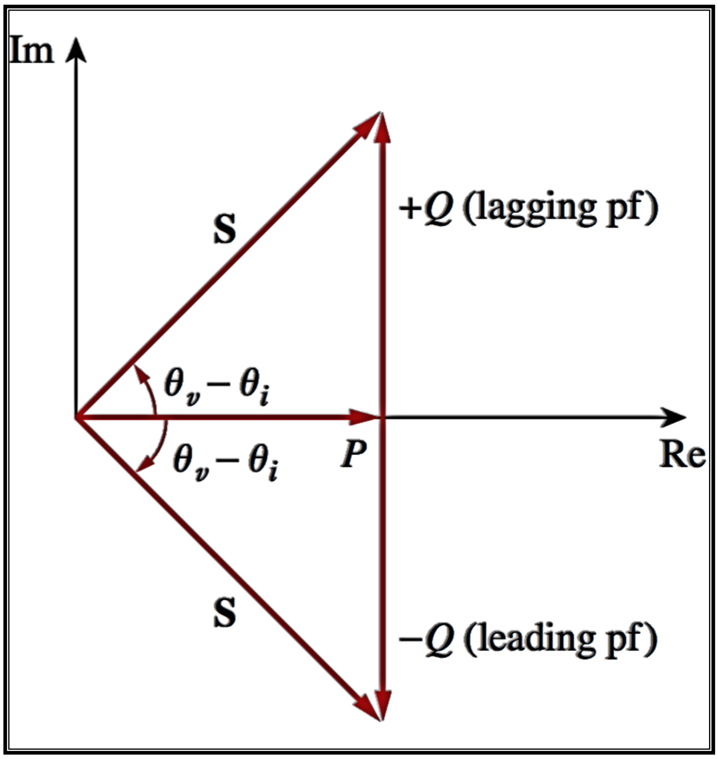


Figure 3.

As shown in Figure 3, when S lies in the first quadrant, **we have an inductive load and a lagging PF**. When S lies in the fourth quadrant, the load is capacitive and the PF is leading. It is also possible for the complex power to lie in the second or third quadrant.

This requires that the load impedance have a negative resistance, which is possible with active circuits.

Role of Active Power and Reactive Power

There is an important relationship between active and reactive power and the post below will help to understand that why active power (P) is called true power and reactive power (Q) is called imaginary power.

First understand what is a coil and inductor. Take an iron rod, wrapped (i.e. winding) it with copper wire. It is a coil or you can say inductor, electromagnet etc. If current passes through the copper wire then iron rod gets magnetized. More will be the current, more the magnetism in the iron rod (i.e. more the flux in iron rod & more the magnetic field around it). Or, it can be said that more the current, more the energy stored by the inductor. (Energy stored by the inductor is given by $\frac{1}{2}LI^2$ where 'L' is the inductance of inductor and 'I' is the magnitude of current through the inductor).

Unit-6

Formation of PN junction (without biasing)

When the N-type semiconductor and P-type semiconductor materials are first joined together a very large density gradient exists between both sides of the PN junction. The result is that some of the free electrons from the donor impurity atoms begin to migrate across this newly formed junction to fill up the holes in the P-type material producing negative ions.

However, because the electrons have moved across the PN junction from the N-type silicon to the P-type silicon, they leave behind positively charged donor ions (N_D) on the negative side and now the holes from the acceptor impurity migrate across the junction in the opposite direction into the region where there are large numbers of free electrons.

As a result, the charge density of the P-type along the junction is filled with negatively charged acceptor ions (N_A), and the charge density of the N-type along the junction becomes positive. This charge transfer of electrons and holes across the PN junction is known as diffusion. The width of these P and N layers depends on how heavily each side is doped with acceptor density N_A, and donor density N_D, respectively.

This process continues back and forth until the number of electrons which have crossed the junction have a large enough electrical charge to repel or prevent any more charge carriers from crossing over the junction. Eventually a state of equilibrium (electrically neutral situation) will occur producing a "potential barrier" zone around the area of the junction as the donor atoms repel the holes and the acceptor atoms repel the electrons.

Since no free charge carriers can rest in a position where there is a potential barrier, the regions on either sides of the junction now become completely depleted of any more free carriers in comparison to the N and P type materials further away from the junction. This area around the PN Junction is now called the Depletion Layer.

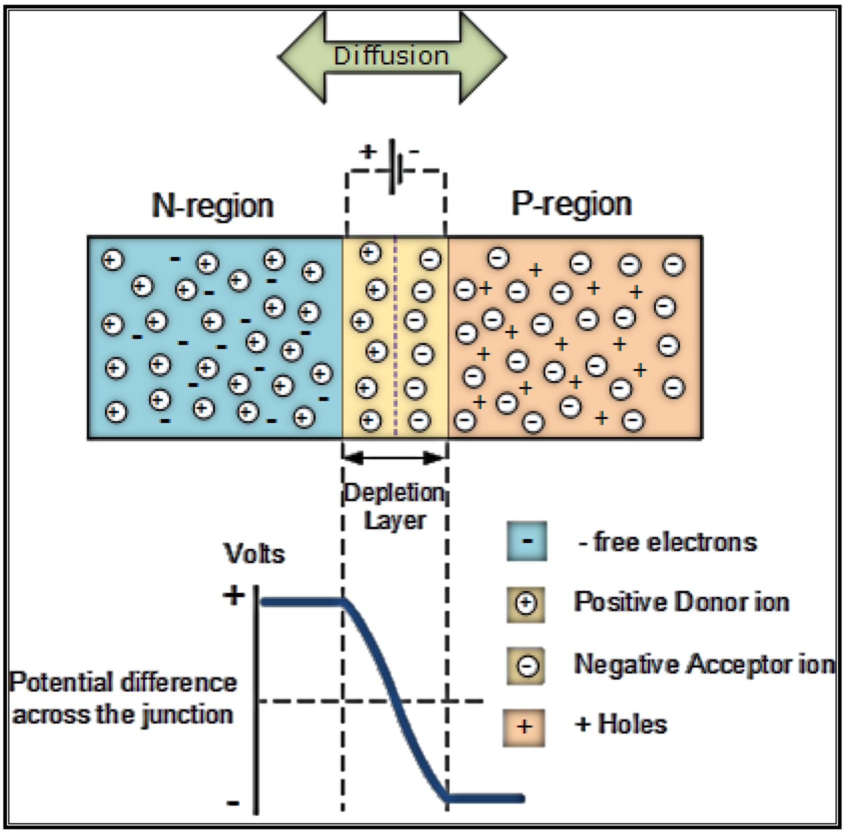


Figure 4.

The total charge on each side of a *PN Junction* must be equal and opposite to maintain a neutral charge condition around the junction. If the depletion layer region has a distance D, it therefore must therefore penetrate into the silicon by a distance of D_p for the positive side, and a distance of D_n for the negative side giving a relationship between the two of: $D_p*N_A = D_n*N_D$ in order to maintain charge neutrality also called equilibrium.

PN Junction Distance

As the N-type material has lost electrons and the P-type has lost holes, the N-type material has become positive with respect to the P-type.

Then the presence of impurity ions on both sides of the junction cause an electric field to be established across this region with the N-side at a positive voltage relative to the P-side. The problem now is that a free charge requires some extra energy to overcome the barrier that now exists for it to be able to cross the depletion region junction.

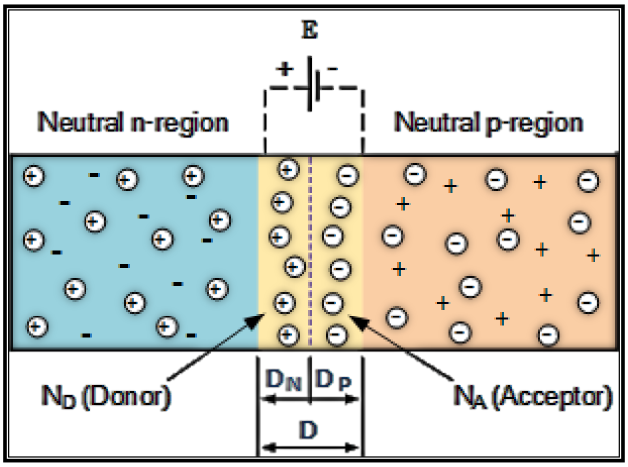


Figure 5.

This electric field created by the diffusion process has created a "built-in potential difference" across the junction with an open-circuit (zero bias) potential of:

$$E_o = V_T \ln\left(\frac{N_D \cdot N_A}{n_i^2}\right)$$

Where: E_o is the zero bias junction voltage, V_T the thermal voltage of 26mV at room temperature, N_D and N_A are the impurity concentrations and n_i is the intrinsic concentration.

A suitable positive voltage (forward bias) applied between the two ends of the PN junction can supply the free electrons and holes with the extra energy. The external voltage required to overcome this potential barrier that now exists is very much dependent upon the type of semiconductor material used and its actual temperature.

Typically at room temperature the voltage across the depletion layer for silicon is about 0.6 – 0.7 volts and for germanium is about 0.3 – 0.35 volts. This potential barrier will always exist even if the device is not connected to any external power source, as seen in diodes.

The significance of this built-in potential across the junction, is that it opposes both the flow of holes and electrons across the junction and is why it is called the potential barrier. In practice, a PN junction is formed within a single crystal of material rather than just simply joining or fusing together two separate pieces.

The result of this process is that the PN junction has rectifying current–voltage (IV or I–V) characteristics. Electrical contacts are fused onto either side of the semiconductor to enable an electrical connection to be made to an external circuit. The resulting electronic device that has been made is commonly called a PN junction Diode or simply Signal Diode.

Then we have seen here that a PN junction can be made by joining or diffusing together differently doped semiconductor materials to produce an electronic device called a diode which can be used as the basic semiconductor structure of rectifiers, all types of transistors, LED's, solar cells, and many more such solid state devices.

PN Junction Diode (with biasing)

If we make electrical connections at the ends of both the N-type and the P-type materials and then connect them to a battery source, an additional energy source now exists to overcome the potential barrier.

The effect of adding this additional energy source results in the free electrons being able to cross the depletion region from one side to the other. The behaviour of the PN junction with regards to the potential barrier's width produces an asymmetrical conducting two terminal device, better known as the **PN Junction Diode**.

A *PN Junction Diode* is one of the simplest semiconductor devices around, and which has the characteristic of passing current in only one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as the diode has an exponential current-voltage (I-V) relationship and therefore we can not described its operation by simply using an equation such as Ohm's law.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased.

By applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking current flow through the diode.

Then the depletion layer widens with an increase in the application of a reverse voltage and narrows with an increase in the application of a forward voltage. This is due to the differences in the electrical properties on the two sides of the PN junction resulting in physical changes taking place. One of the results produces rectification as seen in the PN junction diodes static I-V (current-voltage) characteristics. Rectification is shown by an asymmetrical current flow when the polarity of bias voltage is altered as shown below.

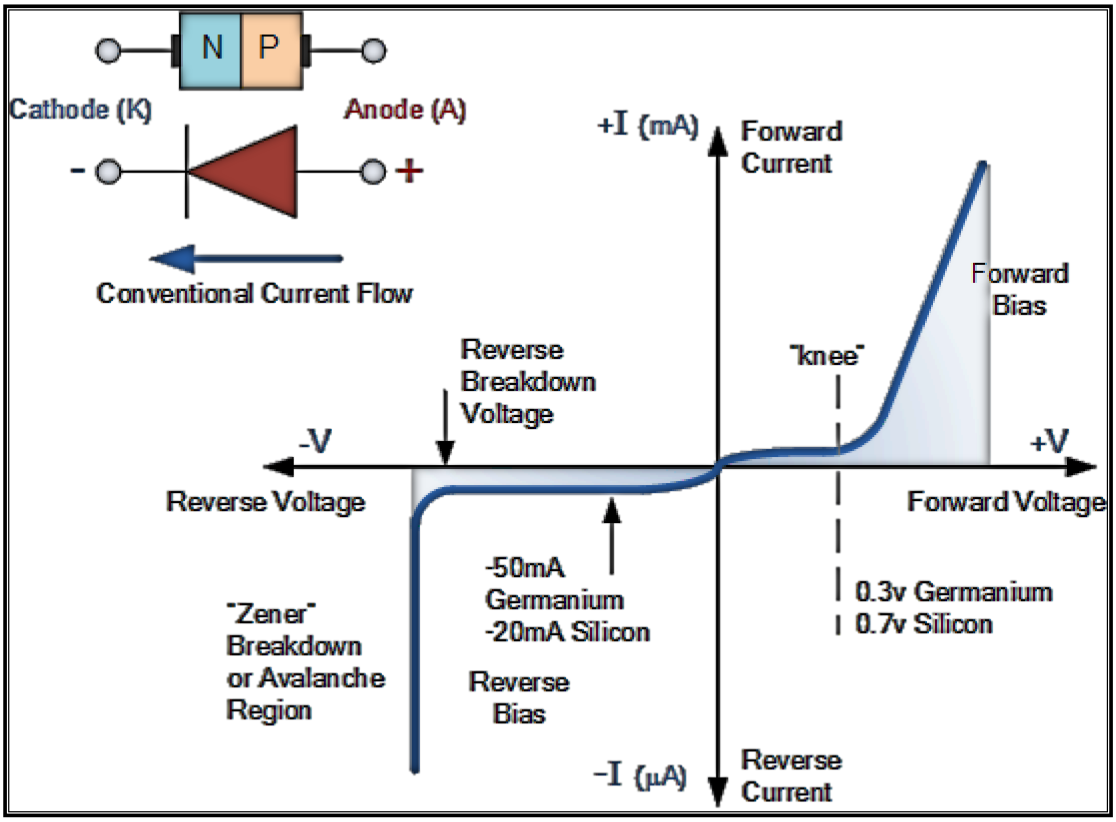


Figure 6.

Let us discuss the biasing ways and the behaviour of the diode in the respective zone. There are two operating regions and three possible "biasing" conditions for the standard **Junction Diode** and these are:

- Reverse Bias – The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of **Increasing** the PN junction diode's width.
- Forward Bias – The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of **Decreasing** the PN junction diodes width.

Reverse Biased PN Junction Diode

When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material.

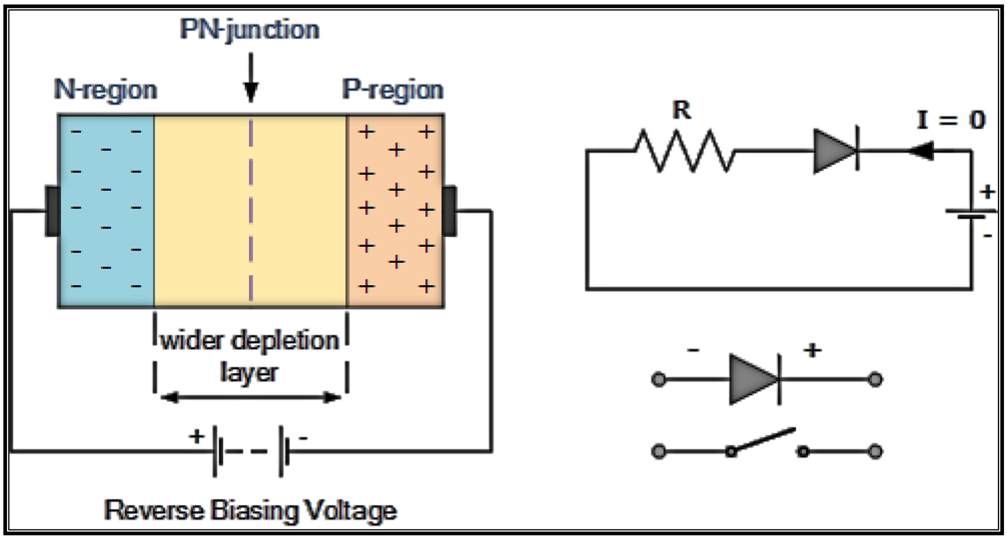


Figure 7.

The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.

The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction which can be measured in micro-amperes, (μA).

One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the diode's PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.

Sometimes this avalanche effect has practical applications in voltage stabilising circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as Zener Diodes.

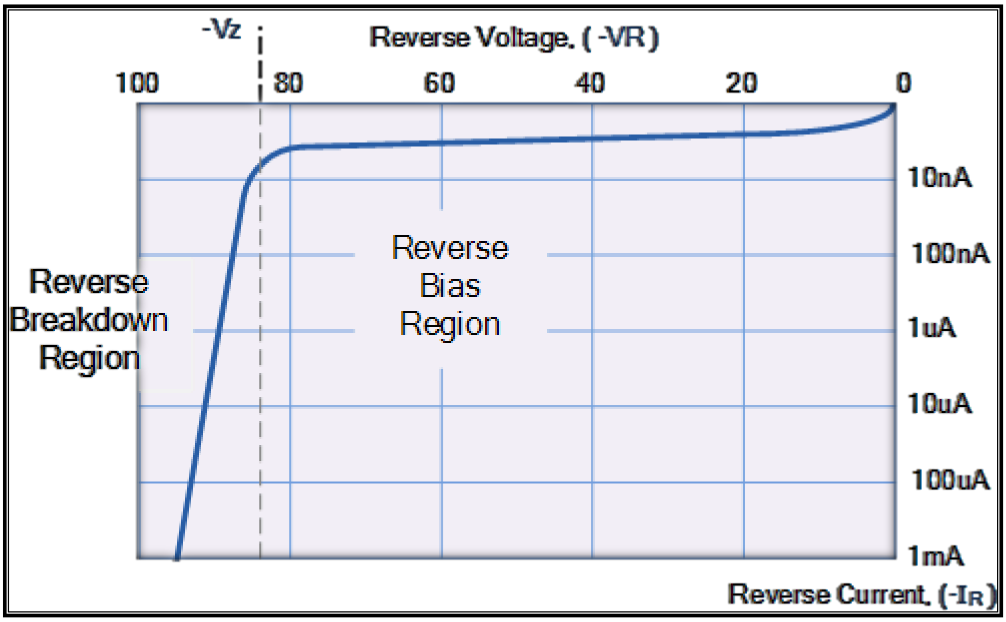


Figure 8.

Forward Biased PN Junction Diode

When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow.

This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the “knee” on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the “knee” point.

This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes.

Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow.

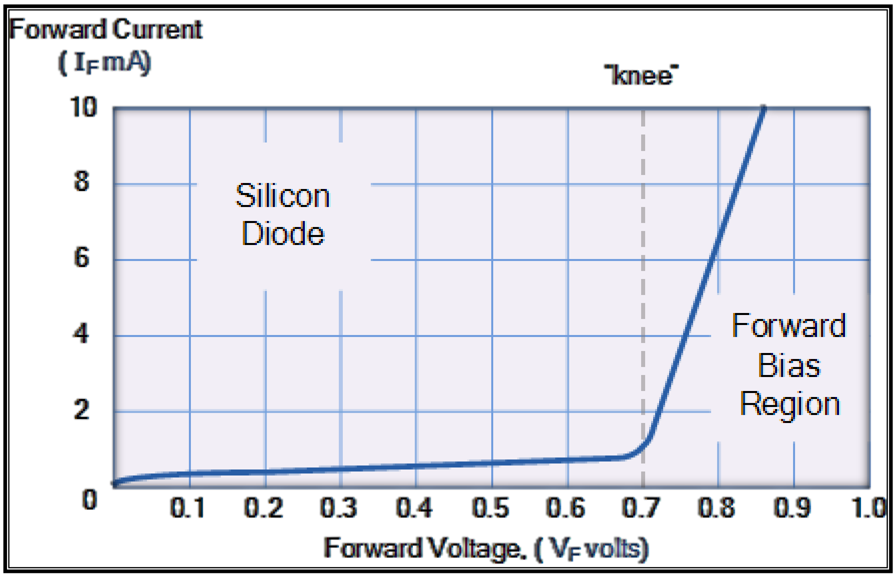


Figure 9.

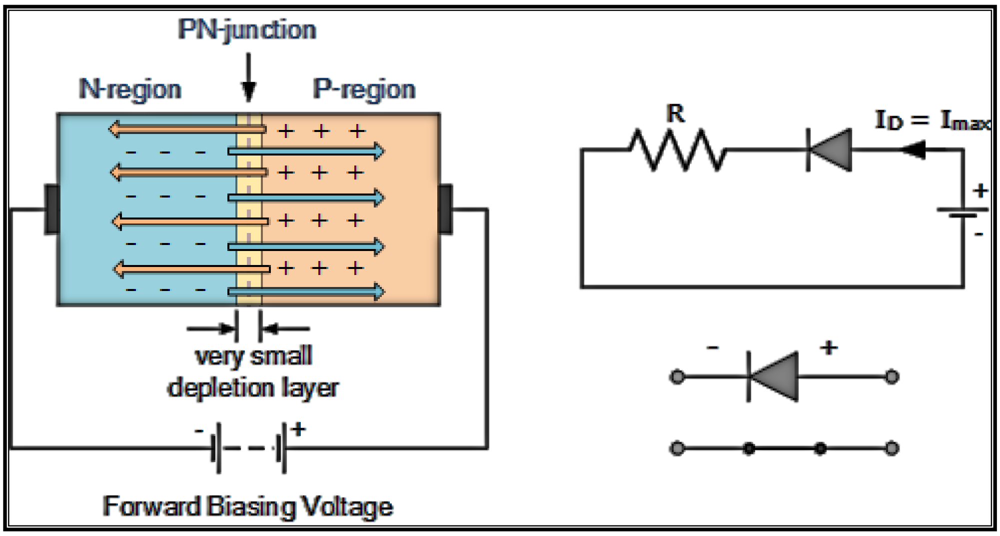


Figure 10.

. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

Junction Diode Summary

The PN junction region of a **Junction Diode** has the following important characteristics:

- Semiconductors contain two types of mobile charge carriers, "Holes" and "Electrons".

- The holes are positively charged while the electrons negatively charged.
- A semiconductor may be doped with donor impurities such as Antimony (N-type doping), so that it contains mobile charges which are primarily electrons.
- A semiconductor may be doped with acceptor impurities such as Boron (P-type doping), so that it contains mobile charges which are mainly holes.
- The junction region itself has no charge carriers and is known as the depletion region.
- The junction (depletion) region has a physical thickness that varies with the applied voltage.
- When a diode is **Zero Biased** no external energy source is applied and a natural **Potential Barrier** is developed across a depletion layer which is approximately 0.5 to 0.7v for silicon diodes and approximately 0.3 of a volt for germanium diodes.
- When a junction diode is **Forward Biased** the thickness of the depletion region reduces and the diode acts like a short circuit allowing full current to flow.
- When a junction diode is **Reverse Biased** the thickness of the depletion region increases and the diode acts like an open circuit blocking any current flow, (only a very small leakage current).